



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,823	03/12/2004	Hyeon-Yong Jang	YOM-0074	8366
23413 7590 05/14/2007 CANTOR COLBURN, LLP 55 GRIFFIN ROAD SOUTH BLOOMFIELD, CT 06002			EXAMINER TRAN, MY CHAU T	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 05/14/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/799,823	<b>Applicant(s)</b> JANG, HYEON-YONG	
	<b>Examiner</b> MY-CHAU T. TRAN	<b>Art Unit</b> 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 23 April 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18, 20 and 21 is/are rejected.
- 7) ☒ Claim(s) 19 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Application and Claims Status***

1. Applicant's amendment and response filed 04/23/2007 are acknowledged and entered.
2. Claims 1-21 were pending. Applicants have amended claims 1, 12, and 13. No claims were added and/or cancelled. Therefore, claims 1-21 are currently pending and are under consideration in this Office Action.

***Status of Claim(s) Objection(s) and /or Rejection(s)***

3. The rejections of claim 16 under 35 USC 112, second paragraph, as being indefinite has been withdrawn in light of applicant's amendments of claim 1.
4. The rejection of claims 1 and 9 under 35 USC 102(b) as being anticipated by Tsunoda et al. (US Patent 5,912,713) has been withdrawn in view of applicant's amendments of claim 1.
5. The rejection of claims 1-16 under 35 USC 103(a) as being obvious over Tanaka et al. (US Patent 6,011,534) in view of Jefferson (US Patent 6,127,865) has been withdrawn in light of applicant's amendments of claim 1.

***Maintained Rejection(s)***

***Claim Rejections - 35 USC § 103***

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Claims 17, 18, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (US Patent 6,011,534) in view of Jefferson (US Patent 6,127,865).

Tanaka et al. disclose a driving circuit for image display device such as a liquid crystal device (see e.g. Abstract; col. 1, lines 8-15; col. 6, lines 13-23). The driving circuit includes a PLL circuit (ref. # 2 of fig. 1), which receive signals based on a horizontal synchronizing signal, i.e. HSYN, and a vertical synchronizing signal, i.e. VSYN, of an input composite signal, i.e. CSYN, (refers to instant claimed input terminals)(see e.g. col. 6, lines 13-23; fig. 1). As illustrated by figure 1, PLL circuit comprises a phase comparator (ref. #2a), an integrator (ref. #2b), a voltage control oscillator (ref. #2c) and a divider (ref. #2d)(see e.g. col. 6, line 66 thru col. 7, line 10). The phase comparator compares the phases of the horizontal synchronization signal and the signal from the divider and generates an output signal of which value is determined based on the comparison (see e.g. fig. 1). The integrator generates a voltage signal having a magnitude proportional to an integration of the output signal of the phase comparator (see e.g. col. 7, lines 5-7; fig. 1). The voltage control oscillator generates a signal in response to the output signal of the phase comparator (see e.g. col. 7, lines 1-9; fig. 1).

For *claims 17 and 18*, Tanaka et al. disclose a driving method that comprises the step of (a) generating a signal having a frequency, (b) detecting the phase difference between the horizontal synchronizing signal and the generated signal by comparing these signals, (c) integrating the compare signals to generate a detected signal, (d) adjusting the frequency of the reference signal in response to the detected signal, and (d) providing a driving signal to a light source (see e.g. col. 6, lines 24-38; col. 7, lines 1-12; fig. 1).

The teachings of Tanaka et al. differs from the presently claimed invention as follows:

For **claim 20**, Tanaka et al. fail to disclose the step of (a) performing pulse width modulation with respect to the reference signal to generate a modulated signal, and (b) dividing a frequency of the modulated signal to generate a frequency-divided signal.

For **claim 21**, Tanaka et al. fail to disclose the step of filtering out high frequency components of the result signal obtained from the comparing step.

However, Jefferson teaches the limitations that are deficient in Tanaka et al.

Jefferson discloses a logic device that includes a PLL system (ref. #62 of fig. 3)(see e.g. col. 5, line 41 thru col. 7, line 11). The PLL system as illustrated by figure 3 includes a phase frequency detector (ref. #68 of fig. 3), a low pass filter (ref. #70 of fig. 3), a voltage control oscillator (ref. #66 of fig. 3), a delay element (ref. #72 of fig. 3), a divide-by-two circuit (ref. #74 of fig. 3), and a multiplexer (ref. #75 of fig. 3)(see e.g. col. 5, line 61 thru col. 7, line 11).

For **claims 20 and 21**, Jefferson discloses that the divide-by-two circuit (refers to instant claimed frequency divider) divides the output signal from the delay element to produce a frequency- divided signal such that the frequency of the modulated signal is twice a frequency of the frequency-divided signal (see e.g. col. 5, lines 64-65; col. 8, lines 44-53).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to disclose the limitations of claims 1, 9-12, 15, 20, and 21 as discussed above that is taught by Jefferson in the device of Tanaka et al. One of ordinary skill in the art would have been motivated to disclose the limitations of claims 1, 9-12, 15, 20, and 21 as discussed above in the device of Tanaka et al. for the advantage of providing a device that can receive two different phase shift signals (Jefferson: col. 3, lines 35-41). Furthermore, one of ordinary skill in the art would have a reasonable expectation of success in the combination of

Tanaka et al. and Jefferson because the PLL system of both Tanaka et al. and Jefferson is use to produce a clock signal from two different phase shift signals.

Therefore, the combine teachings of Tanaka et al. and Jefferson do render the apparatus and method of the instant claims *prima facie* obvious.

### ***Response to Arguments***

8. Applicant's arguments directed to the above 103(a) rejection were considered but they are not persuasive for the following reasons. Please note that the above rejection has been modified from it original version to more clearly address applicant's newly amended and/or added claims and/or arguments.

[1] Applicant contends that Tanaka et al. do not disclose the method claimed in independent claim 17, i.e. *'In contrast and according to the present invention, the oscillator adjusts the frequency of the reference signal in response to the output signal of the phase difference detecting unit, as recited in independent claim 17'*, and support this contention by referring to col. 7, lines 1-5 of Tanaka et al., which states that *'the voltage control oscillator oscillates a signal at a frequency corresponding to a horizontal synchronizing signal input'*.

This is not found persuasive for the following reasons:

[1] The examiner respectfully disagrees. It is the examiner's position that Tanaka et al. do disclose the method claimed in independent claim 17. First, the instant claimed 17 does not explicitly recite that *'the oscillator adjusts the frequency of the reference signal in response to the output signal of the phase difference detecting unit'*, but rather a broad generic method steps. The instant claim 17 recites the method steps of a) *'generating a reference signal having a frequency'*; b) *'detecting a phase difference between a horizontal synchronization signal for the*

Art Unit: 2629

*image display device and the reference signal to generate a detect signal*'; c) *'adjusting the frequency of the reference signal in response to the detect signal*'; and d) *'providing a driving signal to the light source in response to the adjusted reference signal*'. Second, Tanaka et al. specifically states that *'the voltage control oscillator oscillates a signal at a frequency corresponding to a horizontal synchronizing signal of a composite synchronizing signal input to the phase comparator'*, i.e. the horizontal synchronizing signal is not inputted directly to the voltage control oscillator as asserted by applicant but rather that the horizontal synchronizing signal is input to the phase comparator. As a result, Tanaka et al. do suggest that *'the oscillator adjusts the frequency of the reference signal in response to the output signal of the phase difference detecting unit'* as disclose in col. 7, lines 1-5 and depicted in figure 1.

Therefore, the combine teachings of Tanaka et al. and Jefferson do render the method of the instant claims *prima facie* obvious, and the rejection is maintained.

***New Rejection(s) – Necessitated by Amendment***

***Claim Rejections - 35 USC § 112***

9. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10. Claims 1-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant

Art Unit: 2629

art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The amended claim 1 recites the limitation of “*voltage supplying unit to apply AC voltage synchronized with the modulated signal to the light source so as to drive the light source*” regarding the instantly claimed device. This limitation, which narrows the structural features of the instant claimed device (i.e. the claimed device includes a structure feature of ‘*voltage supplying unit*’ that applies an “*AC voltage synchronized with the modulated signal to the light source so as to drive the light source*”), is not supported by the originally filed specification and/or claims; nor has applicant provided any indication where such support exists (i.e. applicant only states that ‘*Support for the amendments to claims 1, 12 and 13 can be found at least in the claims and specification as originally filed*’). See 37 CFR 1.121 (b)(2)(iii), and the MPEP § 714.02, 3<sup>rd</sup> paragraph, last sentence; MPEP § 2163.02; and MPEP § 2163.06. For example, the instant specification discloses that ‘*The operational amplifier **OP** has a non-inverting terminal (+) connected to a voltage divider including a pair of resistors **R3** and **R4** connected in series between a supply voltage *VDDA* and the ground*’ (see specification, pg. 12, lines 14-16; fig. 4). Additionally, the original claims are silent regarding the structure feature of ‘*voltage supplying unit*’ that applies an “*AC voltage*”. As a result, the limitation of “*voltage supplying unit to apply AC voltage synchronized with the modulated signal to the light source so as to drive the light source*” has no specification or original claim support, and it is considered new matter. If applicants disagree, applicant should present a detailed analysis as to why the claimed subject matter has clear support in the originally filed specification and/or claims.



***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 1 and 9 are rejected under 35 U.S.C. 103(a) as being obvious over Tsunoda et al. (US Patent 5,912,713) in view of Kang et al. (US Patent Application Publication US 2004/0004596 A1).

For *claims 1 and 9*, Tsunoda et al. disclose a display apparatus that comprises a display control apparatus (ref. #1 of figure 1) and a display panel unit (ref. #3 of figure 1)(see e.g. Abstract; col. 1, lines 41-47; fig. 1). The display control apparatus comprises a PLL circuit (ref. #41 of figure 1). In one embodiment as illustrated in figure 3, the PLL circuit comprises a phase comparator (refers to instant claimed a phase difference detecting unit), a low-pass filter, a voltage-controlled oscillator (refers to instant claimed an oscillator), a selector (refers to instant claimed controller), a hold switch (ref. #20)(refers to instant claimed switch circuit), a frequency divider, the arrow with "HD" label (refers to instant claimed input terminal that receive a horizontal synchronization signal), and the reference arrows #33 and 34 (refers to instant claimed input terminal that receive a control signal externally provided)(see e.g. col. 5, lines 52-61; col. 6, line 45 thru col. 7, line 19). The phase comparator receive the HD signal (refers to instant claimed horizontal synchronization signal) and the fv signal (refers to instant claimed modulated signal) and detect a phase difference between these two signals and generate an output signal indicating the phase difference, which is sent to the voltage-controlled oscillator wherein the

oscillator adjusts the frequency of the  $f_{out}$  (refers to instant claimed reference signal) in response to the output signal of the phase comparator so that the HD signal and the  $f_v$  signal are synchronized with each other (see e.g. col. 5, lines 52-65). The selector modulates the reference signal in response to the control signal and output a modulated signal (see e.g. col. 6, lines 45-61). The frequency divider divide a frequency of the modulated signal provided from the controller to generate a frequency- divided signal (see e.g. col. 6, lines 45-61).

The teachings of Tsunoda et al. differs from the presently claimed invention as follows:

For **claim 1**, Tsunoda et al. fail to disclose a voltage supplying unit to apply AC voltage synchronized with the modulated signal to the light source so as to drive the light source.

However, Kang et al. teach the limitations that are deficient in Tsunoda et al. as follows:

For **claim 1**, Kang et al. disclose an apparatus of driving a light source for a display device (see e.g. Abstract; sections: [0002], [0014], [0029]; figs. 4 and 5). The device includes an electricity supplying unit (refers to instant claimed a voltage supplying unit) that applies AC voltage synchronized with the modulated signal to the light source so as to drive the light source (see e.g. sections: [0015], [0072] thru [0076]; figs. 4 and 5).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include a voltage supplying unit to apply AC voltage synchronized with the modulated signal to the light source so as to drive the light source as taught by Kang et al. in the device of Tsunoda et al. One of ordinary skill in the art would have been motivated to include a voltage supplying unit to apply AC voltage synchronized with the modulated signal to the light source so as to drive the light source in the device of Tsunoda et al. for the advantage of providing appropriate control of the lamp such that the stability of the lamp is increase (Kang:

Art Unit: 2629

[0083]). Furthermore, one of ordinary skill in the art would have a reasonable expectation of success in the combination of Tsunoda et al. and Kang et al. because the control device of both Tsunoda et al. and Kang et al. is use for driving a liquid crystal display device.

Therefore, the combine teachings of Tsunoda et al. and Kang et al. do render the device of the instant claims *prima facie* obvious.

#### ***Allowable Subject Matter***

13. Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

14. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

Art Unit: 2629


however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MY-CHAU T. TRAN whose telephone number is 571-272-0810. The examiner can normally be reached on Monday: 8:00-2:30; Tuesday-Thursday: 7:30-5:00; Friday: 8:00-3:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

My-Chau T. Tran  
May 7, 2007



RICHARD HJERPE  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600